

DMF 5000 SERIES

USERS MANUAL

OCTOBER 1996

OPTREX CORPORATION

DMF 5000

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1. Outline of LCD Module

The DMF 5000 series dot matrix graphic LCD modules include an LCD controller, a display RAM, a character generator ROM, and drive circuits. These modules are suitable for copiers, facsimiles, PBXs, marine instruments, and messaging displays for various instruments.

1.1 Features

1. Excellent readability and high contrast ratio.
2. bit parallel bus interface.
3. Built-in LCD controller T6963C and display RAM (8K byte).
4. Large graphic display.
5. Various attribute functions.
6. Built-in 128 word character generator ROM, and 256 word (max.) character generator RAM.
7. Wide operating temperature range.
8. Compact and easily mountable on any equipment.

2. Specification

2.1 Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Notes
Supply Voltage (Logic)	V _{cc-Vss}	-0.3	7	V	
Supply Voltage (LCD Drive)	V _{cc-Vee}	V _{cc} +0.3	28	V	
	V _{cc-Vadj}	0	28	V	
Input Voltage	V _i	-0.3	V _{cc} +0.3	V	
Operating Temperature	T _{opr}	0	+50	°C	
	T _{opr}	+10	+40	°C	CCT Backlight Type
Storage Temperature	T _{stg}	-20	+60	°C	

Make sure not to exceed above maximum rating values under the worst probable conditions.

2.2 Electrical Characteristics

Item	Symbol	Condition	Standard Value			Unit
			Min.	Typ.	Max.	
Supply Voltage (Logic)	Vcc-Vss	Ta = 25° C	4.75	5	5.25	V
Supply Voltage (LCD Drive)	Vcc-Vee	Ta = 25° C	10		28	V
	Vcc-Vadj	Ta = 25° C	8		26	V
Supply Current	Icc	Ta = 25° C		10	20	mA
	Iee	Ta = 25° C		4	8	mA
Input Voltage "H" Level	ViH	Ta = 25° C	Vcc-2.2		Vcc	V
Input Voltage "L" Level	ViL	Ta = 25° C	0		0.8	V

2.3 LCD Driving Voltage and Connection

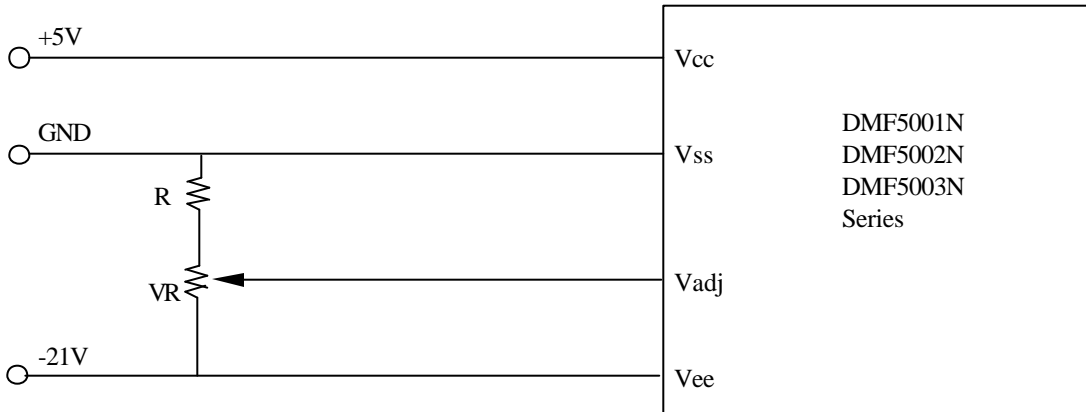
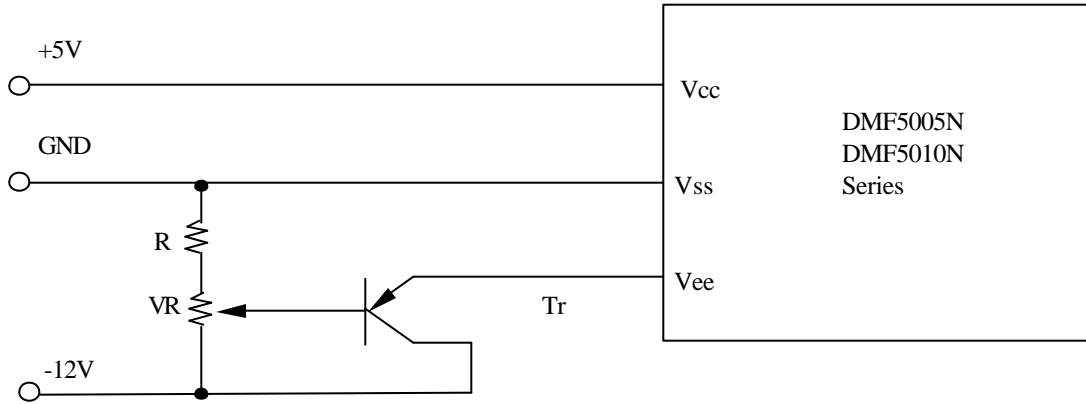
The LCD Panel is driven by the voltage Vcc-Vee or Vcc-Vadj. Adjustable Vee or Vadj is required for contrast control and temperature compensation. Table 2.1 is a recommended power supply voltage for the LCD drive (Vcc-Vee or Vcc-Vadj).

Table 2.1

Temp. Model	0 °C	10 °C	25 °C	40 °C	50 °C	Note
DMF5001N Series (Vcc-Vadj)	23.2V		20.3V		18.3V	1/128 Duty
DMF5002N Series (Vcc-Vadj)	22.4V		19.7V		17.6V	1/112 Duty
DMF5003N Series (Vcc-Vadj)		19.6V	18.4V	17.4V		1/128 Duty CCT Backlight
DMF5005N Series (Vcc-Vee)	14.8V		13.6V		12.3V	1/64 Duty
DMF5010N Series (Vcc-Vee)		14.4V	13.6V	12.8V		1/64 Duty CCT Backlight

Consult your local Optrex representative to obtain detailed specifications for each module part number.

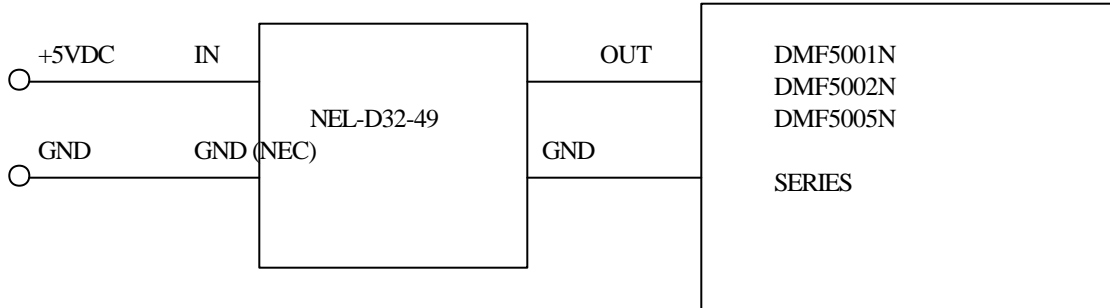
Example of power Supply Connection:



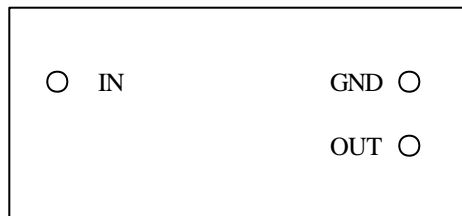
Note: R: $5K\Omega$ - $10K\Omega$
VR: $10K\Omega$ - $20K\Omega$
Tr: 2SA, 1162Y etc.

2.4 EL Back Light

Recommended Inverter and Connection



NEL-D32-49 Specification



Bottom View

Maximum Ratings

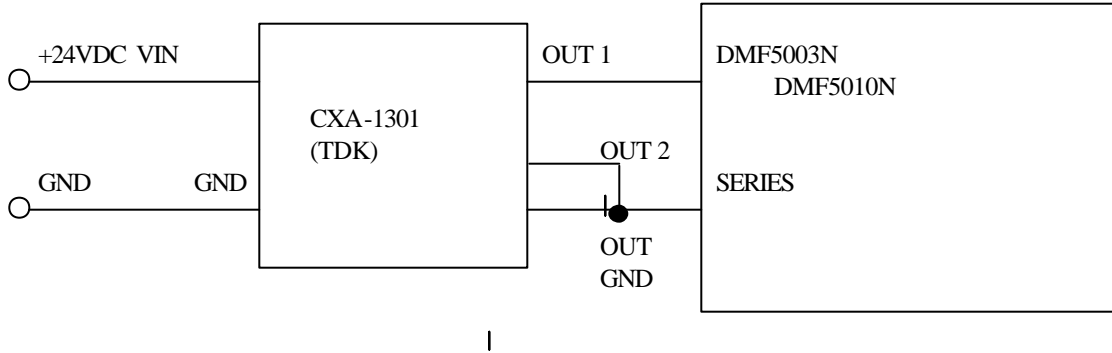
Input Voltage	6VDC
Load (Lamp Surface Area)	95 cm ²
Storage Temperature	-20 - 70°C
Operating Temperature	-10 - 55°C

Acceptable Operating Range

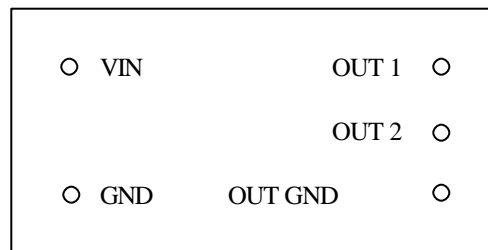
Input Voltage	3-5.5VDC
Load (Lamp Surface Area)	50-83 cm ²

2.5 CCT Back Light

Recommended Inverter and Connection



CXA-1301 Specification



Bottom View

Maximum Ratings

Input Voltage	26.4VDC
Output Power Consumption	5W
Storage Temperature	-20 - 75 °C
Operating Temperature	0 - 50 °C

Acceptable Operating Range

Input Voltage	24±1.2VDC
---------------	-----------

3. Interface

3.1 Interface Connection

DMF 5001N, 5002N, 5003N Series

Pin No.	Symbol	Level	Function
1	FG	-	Frame Ground (Connected to Metal Holder)
2	VSS	-	Ground (Signal Ground)
3	VCC	-	Power Supply (Logic, LCD Drive)
4	VADJ	-	Power Supply for LCD Contrast Adjust
5	VEE	-	Power Supply (LCD Drive)
6	$\overline{\text{WR}}$	L	Data Write (Write Data to the Module at "L")
7	$\overline{\text{RD}}$	L	Data Read (Read Data from the Module at "L")
8	$\overline{\text{CE}}$	L	Chip Enable for the Module
9	$\overline{\text{C/D}}$	H/L	WR="L"; C/D="H": Command Write, C/D="L": Data Write RD="L"; C/D="H": Status Read, C/D="L": Data Read
10	$\overline{\text{HALT}}$	L	Stop the Oscillation of Clock
11	$\overline{\text{RESET}}$	L	Controller Reset
12	D ϕ	H/L	Data Input/Output (LSB)
13	D1	H/L	Data Input/Output
14	D2	H/L	Data Input/Output
15	D3	H/L	Data Input/Output
16	D4	H/L	Data Input/Output
17	D5	H/L	Data Input/Output
18	D6	H/L	Data Input/Output
19	D7	H/L	Data Input/Output (MSB)
20	NC	-	No Connection

Pin No.	Symbol	Level	Function
1	FG	-	Frame Ground (Connected to Metal Holder)
2	VSS	-	Ground (Signal Ground)
3	VCC	-	Power Supply (Logic, LCD Drive)
4	VEE	-	Power Supply (LCD Drive)
5	$\overline{\text{WR}}$	L	Data Write (Write Data to the Module at "L")
6	$\overline{\text{RD}}$	L	Data Read (Read Data from the Module at "L")
7	$\overline{\text{CE}}$	L	Chip Enable for the Module
8	$\overline{\text{C/D}}$	H/L	WR="L"; C/D="H": Command Write, C/D="L": Data Write RD="L"; C/D="H": Status Read, C/D="L": Data Read
9	NC	-	No Connection
10	$\overline{\text{RESET}}$	L	Controller Reset
11	D ϕ	H/L	Data Input/Output (LSB)
12	D1	H/L	Data Input/Output
13	D2	H/L	Data Input/Output
14	D3	H/L	Data Input/Output
15	D4	H/L	Data Input/Output
16	D5	H/L	Data Input/Output
17	D6	H/L	Data Input/Output
18	D7	H/L	Data Input/Output (MSB)
19	FS	H/L	Font Size Select "H": 6 x 8 DOT "L": 8 x 8 DOT
20	NC	-	No Connection

EL Back Light Terminal for DMF 5001N, 5002N, 5005N Series

Pin No.	Symbol	Level	Function
21	EL	-	EL Power Supply
22	EL	-	EL Power Supply

CCT Back Light Terminal for DMF 5003N Series

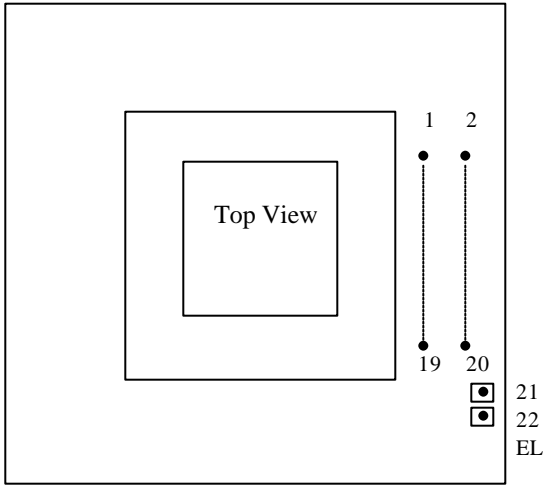
Pin No.	Symbol	Level	Function
1	GND	-	Ground for CCT Power Supply
2	NC	-	No Connection
3	NC	-	No Connection
4	HOT	-	CCT Power Supply

CCT Back Light Terminal for DMF 5010N Series

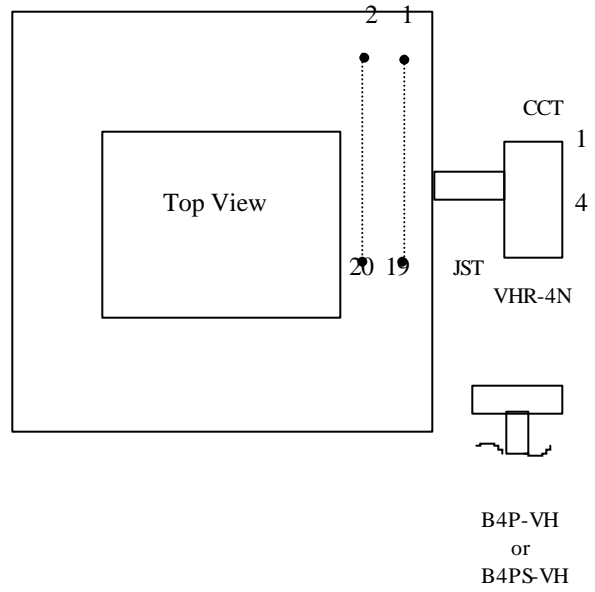
Pin No.	Symbol	Level	Function
1	HOT	-	CCT Power Supply
2	NC	-	No Connection
3	NC	-	No Connection
4	GND	-	Ground for CCT Power Supply

Pin No. Layout

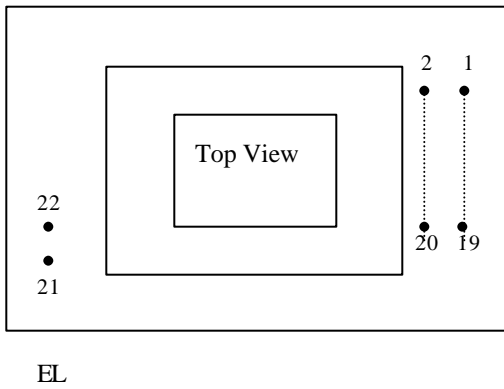
DMF5001N, 5002N Series



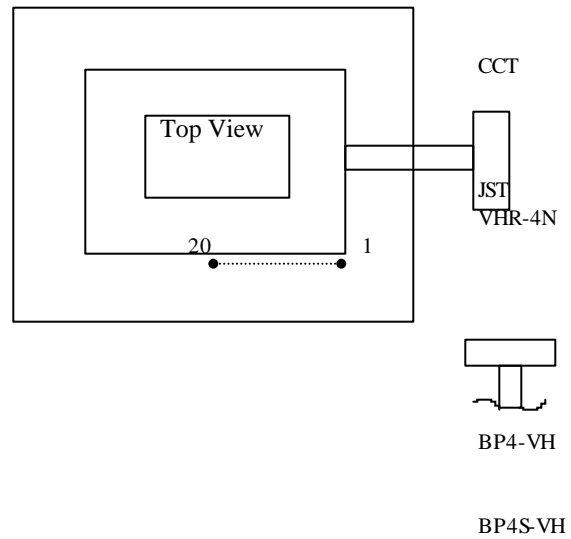
DMF 5003N Series



DMF 5005N Series

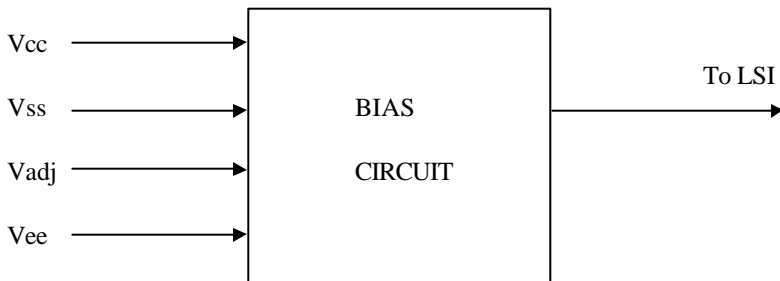
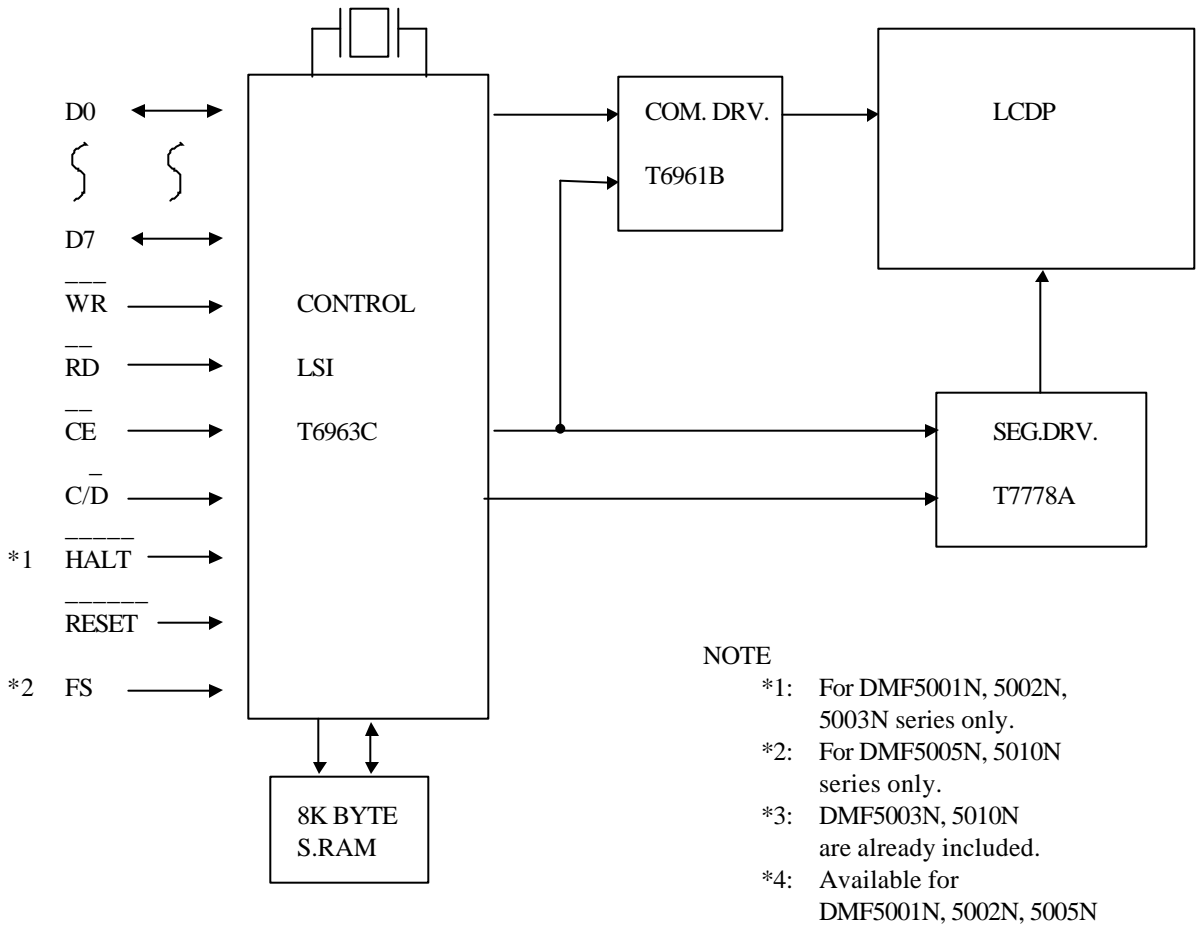


DMF 5010N Series

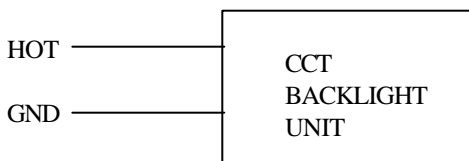


or

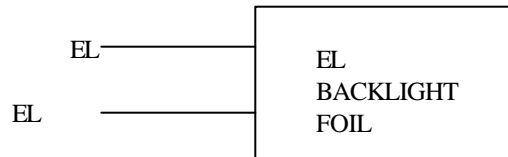
3.2 Block Diagram



*3



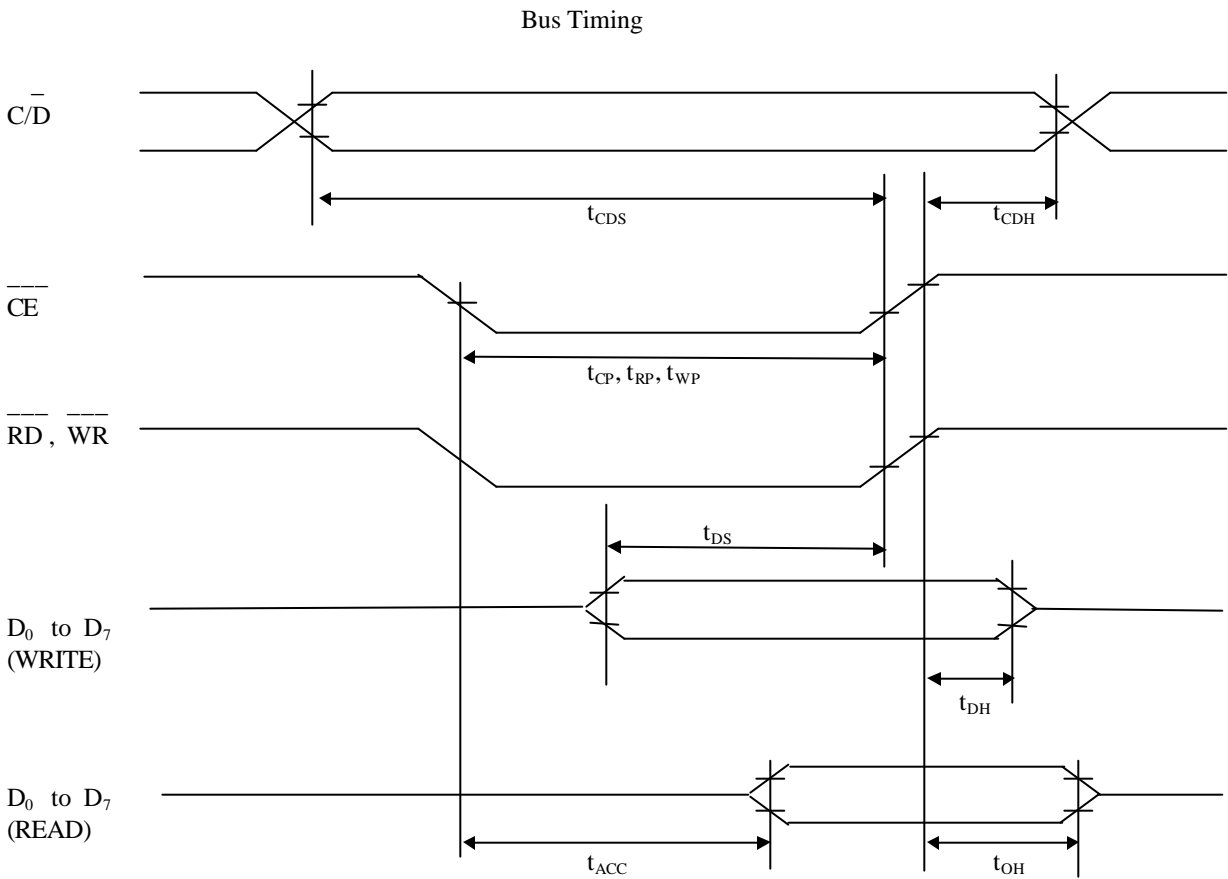
*4



3.3 Signal Timings

Item	Symbol	Min.	Max.	Unit
C/D Set Up Time	t_{CDS}	100	-	ns
C/D Hold Time	t_{CDH}	10	-	ns
CE, RD, WR Pulse Width	t_{CP} , t_{RP} , t_{WP}	80	-	ns
Data Set Up Time	t_{DS}	80	-	ns
Data Hold Time	t_{DH}	40	-	ns
Access Time	t_{ACC}	-	150	ns
Output Hold Time	t_{OH}	10	50	ns

Conditions: $V_{CC} = 5 \pm 0.25V$, $GND = 0V$, $T_a = 25^\circ C$



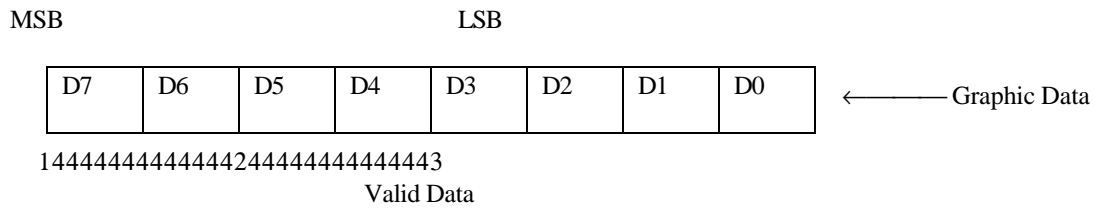
Graphic Display (Ex. 240 x 64 DOT)

TA = 1EH, GA = 1EH
 TH & GH = Within 0000H ~ 1FFFH

GH		TH + 1DH	} 64 Dot
GH + GA		TH + TA + 1DH	
GH + 63GA		TH + 7TA + 1DH	

144444444444444444442444444444444444444443
 30 x 8 = 240 Dot

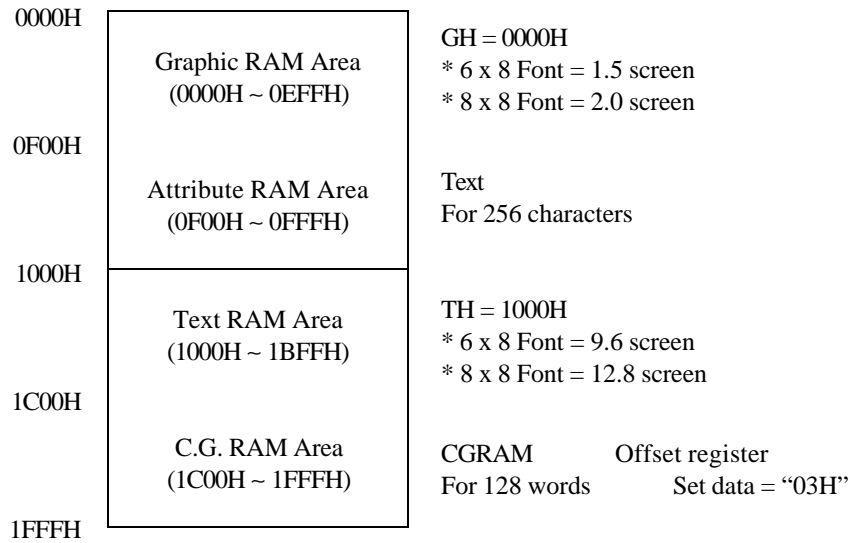
Note: In case of graphic display, 8 bit data is as follows:



3.4.3 RAM Map

The Display RAM is built into the module, and display data is written to this display RAM. The built-in controller LSI/T6963C automatically reads the display RAM and sends the appropriate data to LCD drivers. The “Control Word Set” command (text home set, text area set, etc.) defines the RAM area which is read by the controller LSI making the RAM map programmable by the user. If more than 1 screen can be stored in the RAM. Vertical scrolling and paging is easily performed by resetting text home and/or graphic home address.

DMF5000 series have 8K byte built-in RAM located at address 0000H ~ 1FFFH, and the following is an example of RAM mapping (240 x 64 DOT).



4. Soldering Jumper Setting

4.1 Initial Setting

Initial setting for “Font” and “Column” are described in Table 4.1.

Table 4.1

	Dot	Duty	Bias	Font	Column
DMF5001N Series	160 x 128	1/128	1/12	8 x 8	32 (valid 20)
DMF5002N Series	128 x 112	1/112	1/12	8 x 8	32 (valid 16)
DMF5003N Series	160 x 128	1/128	1/12	8 x 8	32 (valid 20)
DMF5005N Series	240 x 64	1/64	1/9	6 x 8 (FS=H)	64 (valid 40)
DMF5010N Series	240 x 64	1/64	1/9	6 x 8 (FS=H)	64 (valid 40)

4.2 Explanation of Each Soldering Jumper

- * “Column” designate by soldering jumper.
(J6, J7 for DMF5001N, 5002N, 5003N Series.
J2, J3 for DMF 5005N, 5010N Series.)
- * “Character Font” designate by soldering jumper
(J8, J9 for DMF5001N, 5002N, 5003N Series.
F4, FS for DMF5005N 5010N Series.)

DMF5001N, 5002N, 5003N Series

	Column			
	32	40	64	80
J6	H	L	H	L
J7	H	H	L	L

Initial set: J6, J7 = H

DMF5005N, 5010N Series

	Column			
	32	40	64	80
J2	H	L	H	L
J3	H	H	L	L

Initial set: J2 = H, J3 = L

	Character Font			
	5 x 8	6 x 8	7 x 8	8 x 8
J8	H	L	H	L
J9	H	H	L	L

Initial set: J8, J9 = L

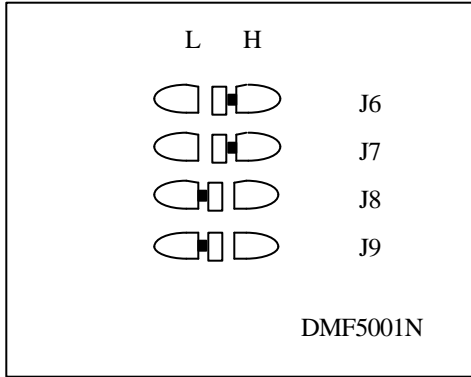
	Character Font			
	5 x 8	6 x 8	7 x 8	8 x 8
J4	H	L	H	L
FS	H	H	L	L

Initial set: J4 = L,
FS = Pull up (H)

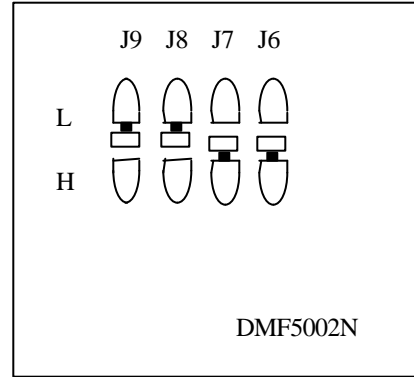
Note: H: +5V (Vcc)
L: 0V (Vss)
FS: I/O terminal pin no. 19 for designate the “Font” from outside of the module.

* Jumper Position

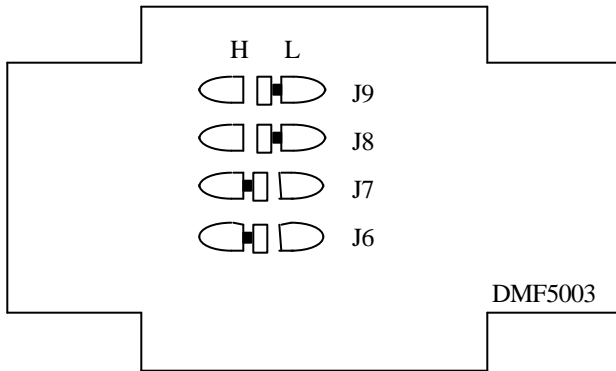
DMF5001N



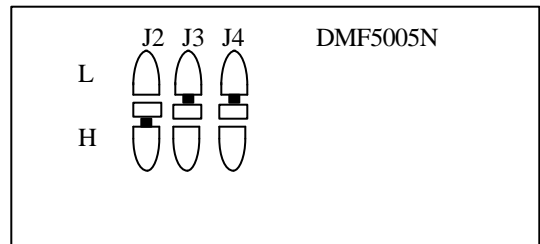
DMF5002N



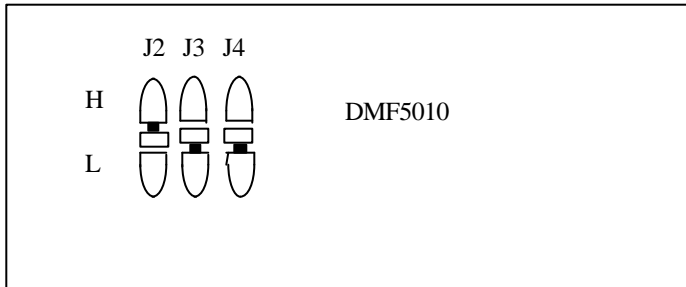
DMF5003N



DMF5005N



DMF5010N



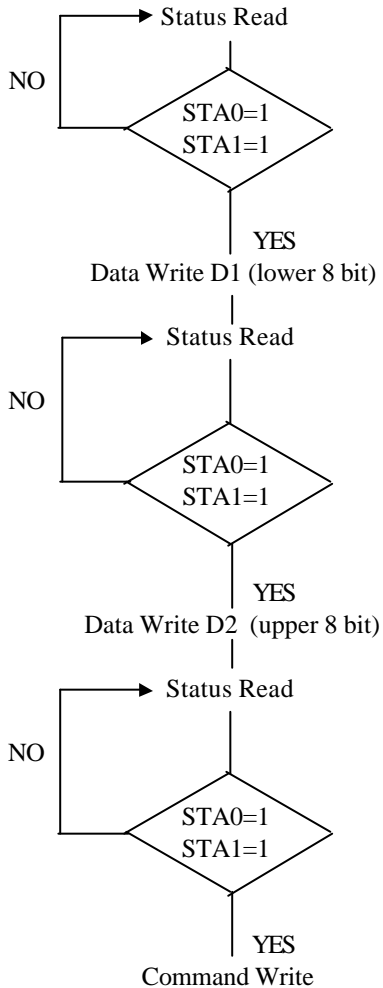
Note: All drawings are PWB's bottom view.

5. Communication between CPU and Module

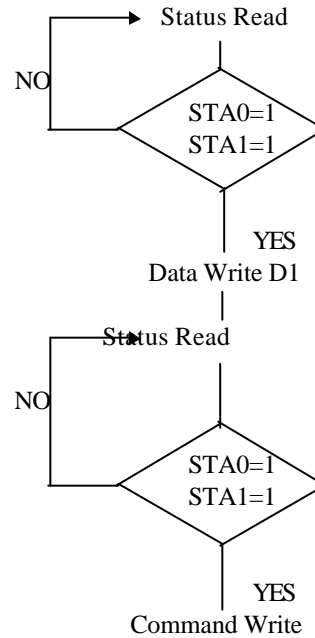
5.1 Data Transmission Method

The built-in LCD controller, T6963C, is operating asynchronously to the CPU clock. The following procedure is required for data transmission between the module and the CPU.

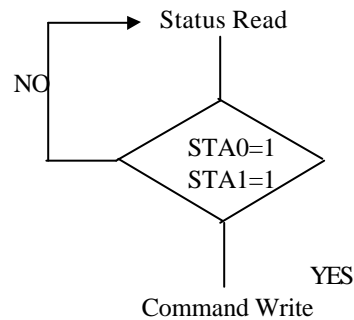
(1) Command with 2 byte data



(2) Command with 1 byte data



(3) Command with no data



(4) Data Auto Write/Data Auto Read

STA2, STA3 should be checked between all data and command.
(Refer 5.2.2.6 “Data Auto Write/Data Auto Read”)

(5) Screen Peeking, Screen Copy

STA6 should be checked just after “Screen Peeking” / “Screen Copy”.
(Refer 5.2.2.8/9 “Screen Peeking”, “Screen Copy”)

5.1.1 Status Read

Status of the controller LSI should be checked between all command and data in order to complete a communication cycle with the CPU. The status can be read from 8 bit data lines (D0 to D7) by setting C/D=“H” and RD=“L”.

STA0 (Busy1)	Check capability of instruction execution.	STA0=0 : Disable =1 : Enable
STA1 (Busy2)	Check capability of data read or data write.	STA1=0 : Disable =1 : Enable
STA2 (DAV)	Check capability of data read (only effective in auto mode.)	STA2=0 : Disable =1 : Enable
STA3 (RDY)	Check capability of data write (only effective in auto mode.)	STA3=0 : Disable =1 : Enable
STA4	–	–
STA5 (CLR)	Check possibility of controller operation.	STA5=0 : Disable =1 : Enable
STA6 (Error)	Address pointer is out of graphic area on screen peeking and screen copy command.	STA6=1 : Out of graphic area
STA7 (Blink)	Check the condition of blink.	STA7=0 : Display off =1 : Normal display (on)

(Status Register)

STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0
MSB				LSB			

5.2 Command

5.2.1 Command List

Command	Command Code								Description	Execution Time (MAX) (Note 1)
	D7	D6	D5	D4	D3	D2	D1	D0		
Pointer Set	0	0	1	0	0	N2	N1	N0	N2 N1 N0 0 0 1 Cursor pointer set 0 1 0 Offset register set 1 0 0 Address pointer set	Status Check
Control Word Set	0	1	0	0	0	0	N1	N0	N1 N0 0 0 Text home address set 0 1 Text area set 1 0 Graphic home address set 1 1 Graphic area set	Status Check
Mode Set	1	0	0	0	CG	N2	N1	N0	CG=0: CG ROM Mode CG=1: CG RAM Mode N2 N1 N0 (Graphic and Text) 0 0 0 "OR" 0 0 1 "EXOR" 0 1 1 "AND" 1 0 0 Text only (attribute capability)	32x1/fOSC
Display Mode	1	0	0	1	N3	N2	N1	N0	N3=0: Graphic display off =1: Graphic display on N2=0: Text display off =1: Text display on N1=0: Cursor display off =1: Cursor display on N0=0: Cursor blink off =1: Cursor blink on	32x1/fOSC
Cursor Pattern Select	1	0	1	0	0	N2	N1	N0	N2, N1, N0 specify the number of cursor lines. (EX) N2 N1 N0	32x1/fOSC

									0 0 0 1 line cursor (bottom line)	
									1 1 1 8 line cursor (8x8 dot cursor)	

Command	Command Code								Description	Execution time (MAX) (Note 1)
	D7	D6	D5	D4	D3	D2	D1	D0		
Data Auto Read/Write	1	0	1	1	0	0	N1	N0	N1 N0 0 0 Data auto write set 0 1 Data auto read set 1 * Auto reset After this command, continuous data can be written or read. (Address pointer automatically increment.)	32x1/fOSC
Data Read/Wrtie	1	1	0	0	0	N2	N1	N0	Data read/write command for 1 byte. N2=0: Address pointer up/down =1: Address pointer unchanged N1=0: Address pointer up =1: Address pointer down N0=0: Data write =1: Data read	32x1/fOSC
Screen Parking	1	1	1	0	0	0	0	0	Transfer display data to data stack for read from CPU.	Status Check
Screen Copy	1	1	1	0	1	0	0	0	1 line displayed data which address is indicated by address pointer is copied to graphic RAM area.	Status Check
Bit Set/Reset	1	1	1	1	N3	N2	N1	N0	Set/reset command for a bit in the address pointed by address pointer. N3=0: Bit reset =1: Bit set N2, N1, N0 indicate the bit in the pointed address. (000 is LSB, and 111 is MSB)	Status Check

Note:

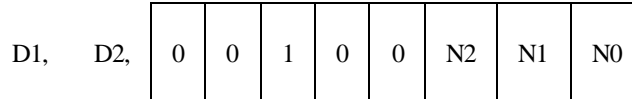
1. Status check between all commands and data is recommended, though execution time for several commands are specified in above command list.

For the commands with “status check” in execution time, execution time is not specified because it is variable depending on the internal operations of the controller LSI.

2. In case of 2 screen mode, Screen copy command cannot be used.

5.2.2 Description of Command

5.2.2.1 Pointer Set Command



Command is selected by setting “1” at selected bit.

N2	N1	N0	Command	D1	D2
0	0	1	Cursor pointer set	Column position	Row Position
0	1	0	Offset register set	Address	00H
1	0	0	Address pointer set	Address (Lower)	Address (Upper)

(a) Cursor Pointer Set

The cursor is displayed at the position specified by the D1, D2. The cursor position is shifted only by this command, and does not shift by other commands. D1, D2 are specified as follows:

D1 : Horizontal cursor position counted by “character” (5 - 8 dot width/character specified by hard setting... refer 4 “Soldering Jumper Setting”). MSB of D1 is neglected, and 127 is the maximum.

D2 : Vertical cursor position counted by “character” (8 dot high character) (1st row of lower half screen is “11H”) Upper 3 bit are neglected and 32 is the maximum.

Note: Please note that the cursor position should be within actual display area.

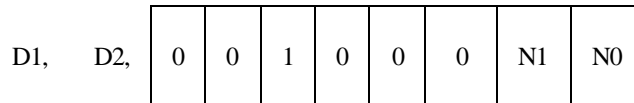
(b) Offset Register Set

The offset register set command is used to determine the character generator RAM area. The upper 5 bits in start address of CG area is set as the lower 5 bits of D1, and the upper 3 bits of D1 are neglected. D2 should be 00H. Refer to section 5.4 “Character Generator” for details of the CG RAM.

(c) Address Pointer Set

The address pointer set command is used to indicate the start address for writing/reading data to/from the built-in RAM. The address should be located in the actual RAM area specified by individual specifications. (Refer to 3.4.3 “RAM MAP”.)

5.2.2.2 Control Word Set Command



Home address of display RAM (Text, Graphic), and areas are defined by this command.

N1	N0	Command	D1	D2
0	0	Text home address set (TH)	Address (Lower)	Address (Upper)
0	1	Text area set (TA)	No. of column	00H
1	0	Graphic home address set (GH)	Address (Lower)	Address (Upper)
1	1	Graphic area set (GA)	No. of column	00H

(a) Text Home Address Set (TH)

This command defines the starting address of display RAM for text display. The data in the text home address (TH) is displayed at the home position of display (left end character on 1st row.)

(b) Text Area Set (TA)

This command defines the number of columns by D1. Text area can be defined independently from the number of characters fixed by hardware setting of controller LSI. The text area is usually defined as the actual number of characters on LCD display, so addressing can be continuous in the text area.

(c) Graphic Home Address Set (GH)

This command defines the starting address of display RAM for the graphic display. The data in the Graphic home address (GH) is displayed at the home position of display (left end 8 bits in 1st line). When using the attribute function, the graphic home address indicates the starting address of distribute RAM area.

(d) Graphic Address Set (GA)

This command defines the number of columns by D1. The graphic area can be defined independently from the number of characters fixed by hardware setting of controller LSI. If the graphic area is defined as the actual number of columns on the LCD display, the address in graphic area can be continuous and the RAM area can be used without ineffective areas. Note that the Graphic area will be different for depending on character font settings even if horizontal dot number is the same.

5.2.2.3 Mode Set Command

(No data)	1	0	0	0	CG	N2	N1	N0
-----------	---	---	---	---	----	----	----	----

Mode set command selects character generator (CG ROM Mode/CG RAM Mode), and combination of text/graphic display.

CG	Command	
0	CG ROM Mode:	Built-in 128 character CG ROM (code: 00H - 7FH) and built-in CG RAM for 128 characters can be used.
1	CG RAM Mode:	Built-in CG RAM for 256 characters (code: 00H - FFH) can be used.

When CG ROM Mode is selected, character code 00H - 7FH is selected from built-in CG ROM and 80H - FFH is automatically selected from CG RAM.

N2	N1	N0	Command
0	0	0	Logically “OR” of Graphic and Text display,
0	0	1	Logically “EXOR” of Graphic and Text display.
0	1	1	Logically “AND” of Graphic and Text display.
1	0	0	Text display only (text can be attributed by the data in the graphic area.)

Logically “OR”, “EXOR”, and “AND” of graphic and text display can be displayed by this command. Only text display is attributed because Attribute RAM is located in Graphic RAM area. (Refer 5.5 “Attribute”)

5.2.2.4 Display Mode Set Command

(No data)	1	0	0	1	N3	N2	N1	N0
-----------	---	---	---	---	----	----	----	----

Display mode is selected from combination of following 4 bits by setting “1” at the selected bit.

	Command
N0	Cursor blink ON (N0=1)/Cursor blink OFF (N0=0)
N1	Cursor display ON (N1=1)/Cursor display OFF (N1=0)
N2	Text display ON (N2=1)/Text display OFF (N2=0)
N3	Graphic display ON (N3=1)/Graphic display OFF (N3=0)

After hard reset, all displays are inhibited. (N0=N1=N2=N3=0)

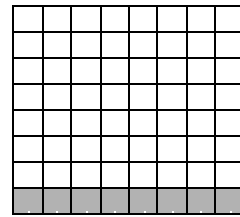
5.2.2.5 Cursor Pattern Select Command

(No data)	1	0	1	0	0	N2	N1	N0
-----------	---	---	---	---	---	----	----	----

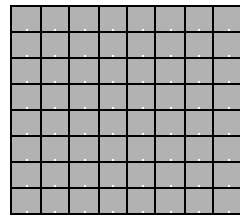
When cursor display is “ON”, this command selects the cursor pattern from 1 line width cursor to 8 line width cursor (block).

N2	N1	N0	Cursor pattern
0	0	0	1 line width cursor
0	0	1	2 line width cursor
0	1	0	3 line width cursor
0	1	1	4 line width cursor
1	0	0	5 line width cursor
1	0	1	6 line width cursor
1	1	0	7 line width cursor
1	1	1	8 line width cursor

(1 line width cursor)



(8 line width cursor)



5.2.2.6 Data Auto Write/Data Auto Read

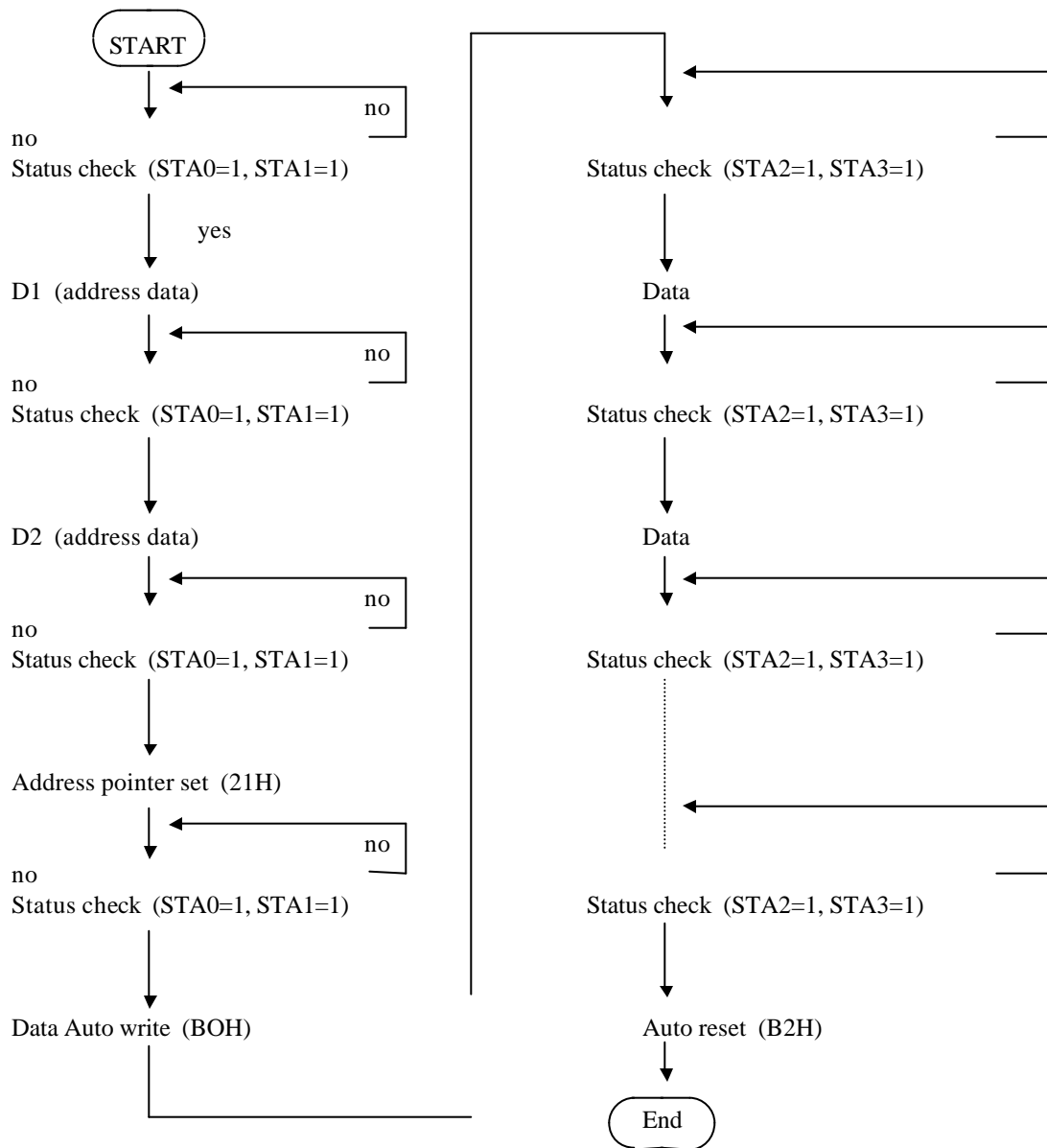
(No data)	1	0	1	1	0	0	N1	N0
-----------	---	---	---	---	---	---	----	----

This command is convenient to send full screen data, or receive full screen data from built-in RAM. After setting auto mode, “data write (or read)” command is not necessary between each data. “Data auto write (or read)” command should follow the “address pointer set” and address pointer is automatically increment by +1 after each data. After sending (or receiving) all data, auto mode reset is necessary to return normal operation because all data is regarded “display data” and no command can be accepted in the auto mode.

N1	N0	Command
0	0	Data Auto Write Set
0	1	Data Auto Read Set
1	*	Auto Mode Reset

*: Don't care.

Note: Status check for auto mode (STA2, STA3) should be checked between each data. Auto reset should be performed after checking STA3=1 (Data Auto Write only). Refer to the following chart.



5.2.2.7 Data Write/Data Read

D1,	1	1	0	0	0	N2	N1	N0
-----	---	---	---	---	---	----	----	----

Note: D1 is necessary only for data write.

This command is used for data write from CPU to built-in RAM, and data read from built-in RAM to CPU. Data write/data read should be executed after setting address by address pointer set command. Address pointer can be automatically increment or decrement by setting this command.

N2	N1	N0	
0	0	0	Data Write (after execution address pointer increment)
0	0	1	Data Read (after execution address pointer increment)
0	1	0	Data Write (after execution address pointer decrement)
0	1	1	Data Read (after execution address pointer decrement)
1	*	0	Data Write (after execution address pointer unchanged)
1	*	1	Data Read (after execution address pointer unchanged)

*: Don't care

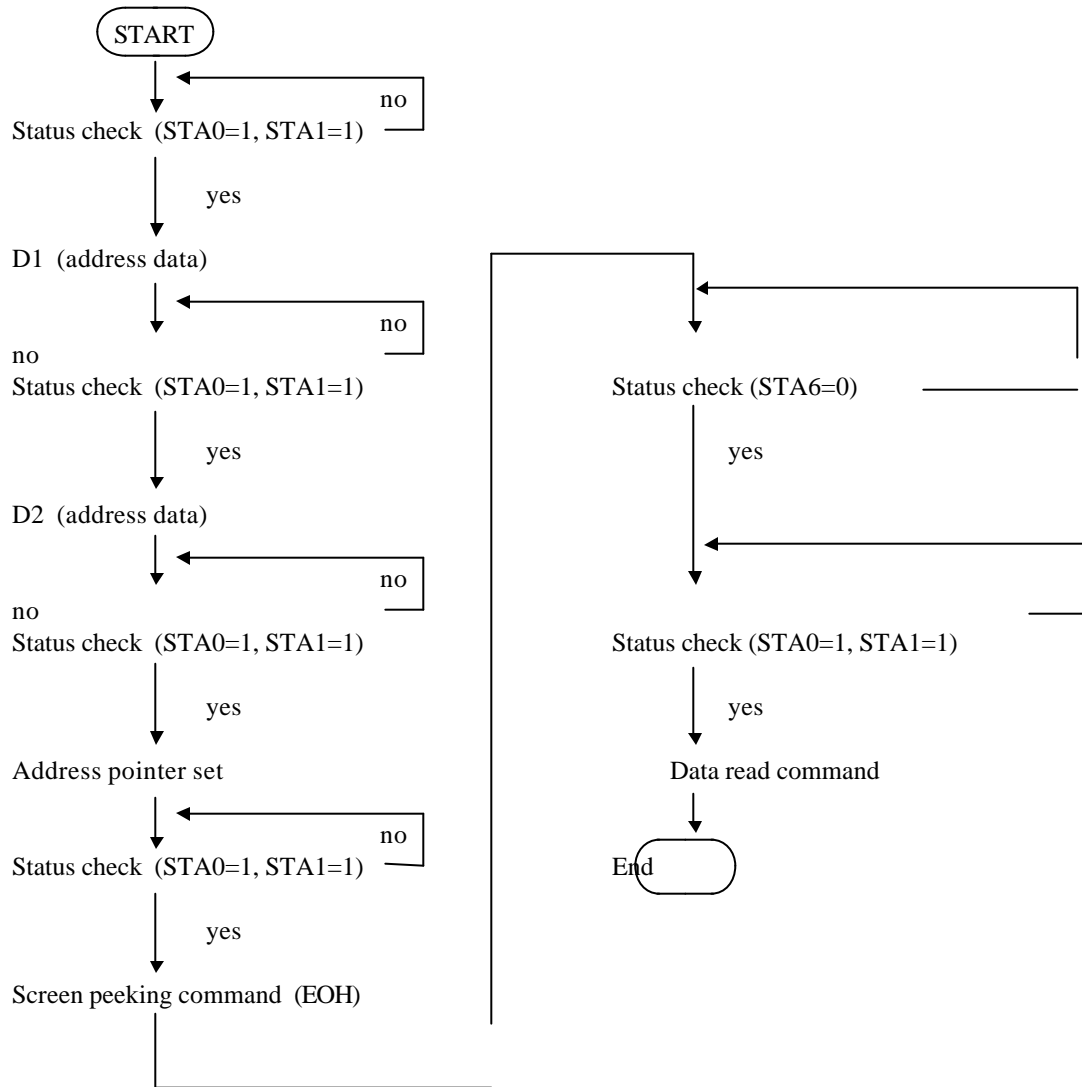
This command is necessary for each 1 byte data.

5.2.2.8 Screen Parking

(No data)	1	1	1	0	0	0	0	0
-----------	---	---	---	---	---	---	---	---

This command is used to transfer displayed 1 byte data to data stack, and this 1 byte data can be read from CPU by data read command. So, logical combination data of text and graphic display on LCD screen can be read by this command. Status (STA6) should be checked just after "screen peeking" command. If the address determined by "address pointer set" command is not in graphic RAM area, this command is ignored and status flag (STA6) is set.

The procedure to read displayed data using this command is as follows:



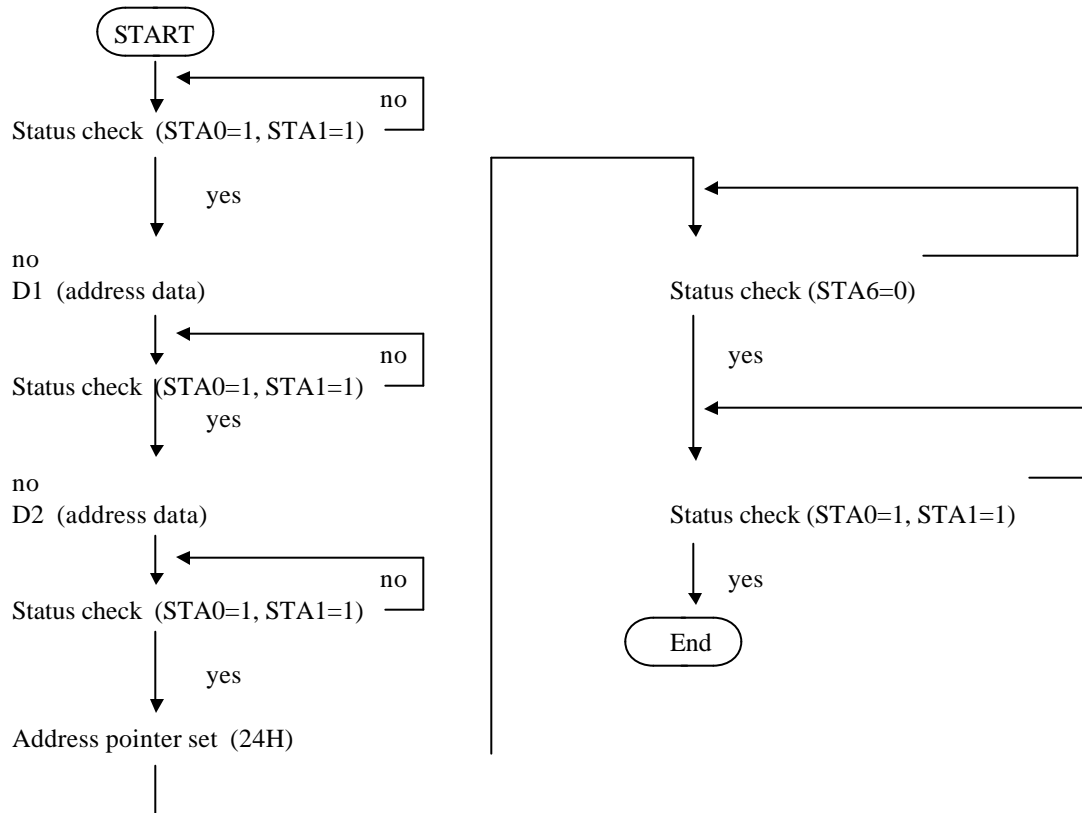
Screen peaking command can be used for getting hard copy of LCD display. Another application of this command is that modified CG is set in the CG RAM area by reading combination data of text and graphic data and writing to CG RAM area. For example, CG for reverse character is made by this method.

5.2.2.9 Screen Copy

(No data)	1	1	1	0	1	0	0	0
-----------	---	---	---	---	---	---	---	---

1 low data displayed in LCD screen can be copied to the graphic RAM area specified by “address pointer set” command. Start point of 1 low data in the screen is determined by the “address pointer set” command. If attribute for text display is set by “Mode Set” command, “screen copy” command can not be used.

Status (STA6) should be checked just after this command. If the address determined by “address pointer set” command is not located in graphic RAM area, this command is ignored and status flag (STA6) is set. The procedure to copy the displayed data using this command is as follows.



Note: In case of 2 screen mode, Screen copy command cannot be used.

5.2.2.10 Bit Set, Bit Reset

(No data)	1	1	1	1	N3	N2	N1	N0
-----------	---	---	---	---	----	----	----	----

One bit in the 1 byte data specified by “address pointer set” command can be set or reset. Plural bits in the 1 byte data cannot be set/reset at a time.

			Description				
N3			N3 = 1 : bit set, N3 = 0 : bit reset				
N2	N1	N0	N2, N1, N0 specify the bit for set/reset.	N2,	N1,	N0	
				0	0	0	bit 0 (LSB)
				0	0	1	bit 1
				0	1	0	bit 2
				:	:	:	
				:	:	:	
				:	:	:	
				1	1	1	bit 7 (MSB)

5.3 Initialize

Initialize of controller LSI T6963C is required for “Mode set”, “Control word set” after power on. Following is the one example of initialize procedure of 240 x 64 dot display.

Command	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Note
Power on	Power on									
Hard reset (Use reset terminal)	RESET="L" (1mSec minimum after Vcc ≥ 4.75V)									
Mode set	1	1	0	0	0	0	0	0	0	“OR” mode
Control word set										Graphic home address command
Graphic home position set (Graphic home position 0000H)	0	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	0	
	1	0	1	0	0	0	0	1	0	
Number of graphic area set (Graphic 30 x 8 dots)	0	0	0	0	1	0	1	1	1	Number of area Command
	0	0	0	0	0	0	0	0	0	
	1	0	1	0	0	0	0	1	1	
Text home position set (Text home position 1000H)	0	0	0	0	0	0	0	0	0	Text home address Command
	0	0	0	0	1	0	0	0	0	
	1	0	1	0	0	0	0	0	0	
Number of text area set (Text 30 column)	0	0	0	0	1	0	1	1	1	Number of area Command
	0	0	0	0	0	0	0	0	0	
	1	0	1	0	0	0	0	0	1	
(Initialize end) (Data write)										
Address pointer set (Address pointer 0000H)	0	0	0	0	0	0	0	0	0	Graphic home address Command
	0	0	0	0	0	0	0	0	0	
	1	0	0	1	0	0	1	0	0	
Data write (Graphic)	0	0	1	0	1	0	1	0	1	Data Command
	1	1	1	1	0	0	0	0	0	
	0	1	0	1	0	1	0	1	0	Data Command
	1	1	1	1	0	0	0	0	0	
Address pointer set (Address pointer 1000H)	0	0	0	0	0	0	0	0	0	Text home address Command
	0	0	0	0	1	0	0	0	0	
	1	0	0	1	0	0	1	0	0	
Data write (Text) (o)	0	0	0	1	0	1	1	1	1	Data Command
	1	1	1	0	0	0	0	0	0	
(p)	0	0	0	1	1	0	0	0	0	Data Command
	1	1	1	0	0	0	0	0	0	
Display Mode Set (Text/Graphic on)	1	1	0	0	1	1	1	0	0	

Note:

1. “Status check” should be inserted between all command and data.

Display mode set register is cleared (no display mode) by the hard reset, and no display is appeared on LCD panel. And just after “Display Mode set 9CH”, written data is displayed on the LCD.

5.4 Character Generator

5.4.1 Character Generator ROM

Character generator ROM for 128 characters is built-in this module.

Character code map

ROM Code 0101

LSO \ ASO	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		!	"	#	\$	%	&	'	()	*	+	,	-	.	/
1	@	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
2	a	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
3	P	Q	R	S	T	U	W	X	Y	Z	[\]	^	_	
4	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
5	p	q	r	s	t	u	v	w	x	y	z	{		}	~	
6	ç	û	ë	â	ä	å	ä	ç	è	é	ê	ë	ì	í	î	ä
7	é	æ	Æ	ö	ø	ö	û	ü	ý	ö	ó	ø	é	æ	Æ	é

5.4.2 User Character Generator RAM

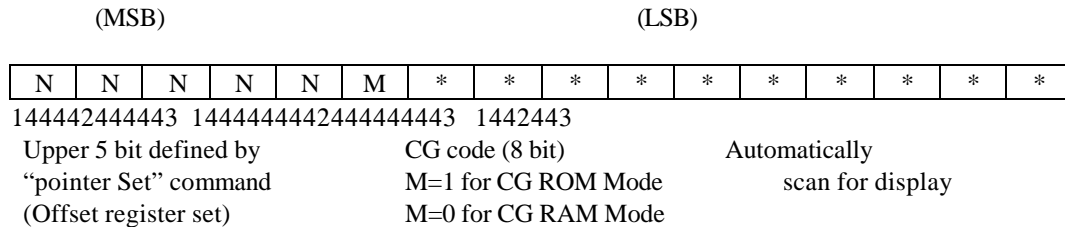
The character generator RAM is the built-in RAM which can be used as character generator after writing character pattern by program. The part of built-in RAM can be used as “User CG RAM” for 256 characters by selecting “CG RAM Mode”, or for 128 characters by selecting “CG ROM Mode”.

1) Position of User CG RAM

The upper 5 bits in start address of User CG RAM (NNNNN) is defined by “Pointer Set” command (Offset register set), and following 2048 byte are defined as “User CG RAM” area when CG RAM Mode is selected. 1024 byte (address: NNNNN10000000000 - NNNNN11111111111) is defined as “User CG RAM” area when CG ROM Mode is selected.

2) Writing to User CG RAM

Character pattern of specified CG code can be written in the pointed address by “Pointer Set” command (Address pointer set). 8 byte data should be sent to following 8 byte address for 1 character.



3) Display Pattern in User CG RAM

Character pattern can be displayed by sending CG code with “Data Write” command. But “Display Mode Set” for text display should be selected before using CG. In case that “CG ROM Mode” is selected, character pattern is selected from built-in CG ROM when MSB=1 (00H - 7FH), and from User CG RAM when MSB=0 (80H-FFH). In case that “CG RM Mode” is selected, all character patterns are selected from User CG RAM (00H-FFH).

4) Relation between User CG RAM Address and CG code and Character Pattern.

When character pattern is written to User CG RAM, relation between CG code and “User CG RAM” address is shown in the following chart:

Character Code 7 6 5 4 3 2 1 0	RAM Address for User CG F E D C B A 9 8 7 6 5 4 3 2 1 0	Character Pattern 7 6 5 4 3 2 1 0
M 0 0 0 0 0 0 0	N N N N N M 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
		0 0 1
		0 1 0
		0 1 1
		1 0 0
		1 0 1
		1 1 0
		1 1 1
M 0 0 0 0 0 0 1	N N N N N M 0 0 0 0 0 0 1 0 0 0 0 0	0 1 0 0 0 0 1 0
		0 1 1 0 0 1 1 0
		0 1 0 1 1 0 1 0
		0 1 0 1 1 0 1 0
		0 1 0 0 0 0 1 0
		0 1 0 0 0 0 1 0
		0 1 0 0 0 0 1 0
		0 0 0 0 0 0 0 0
M 0 0 0 0 0 1 0	N N N N N M 0 0 0 0 0 1 0 0 0 0 0 0	0 1 0 0 0 0 1 0
		0 1 1 0 0 0 1 0
		0 1 0 1 0 0 1 0
≈	≈	≈
1 1 1 1 1 1 1 1	N N N N N 1 1 1 1 1 1 1 1 0 0 0 0	0 1 1 1 0 0 0 0
		0 1 0 0 0 0 0 0
		0 1 1 1 1 0 1 0
		0 0 0 1 1 0 1 0
		0 1 1 1 1 0 1 0
		0 0 0 0 1 1 1 0
		0 0 0 0 1 0 1 0
		0 0 0 0 1 0 1 0

Note 1:

Character code in “User CG RAM” is located from 80H to FFH in case of “CG ROM Mode”, and from 00H to FFH in case of “CG RAM Mode”. So, M in above chart is as follows:

M=1 : “CG ROM Mode”

M=0 : “CG RAM Mode”

Note 2:

“NNNNN” is the upper 5 bits in start address of User CG RAM defined by “Pointer Set” command (Offset Register Set).

Note 3:

It must be careful so that User CG RAM area should not be rewritten by display data, etc.

5.5 Attribute

5.5.1 Attribute Function

This module has attribute function for “Reverse display”, “Blink” in text display mode. Attribute data is written in the “Graphic area” defined by “Control word set” command (Graphic home address set and Graphic area set). So “Text display only” Mode should be selected by “Mode Set” command, and graphic display cannot be displayed.

The attribute data of the 1st character in “Text area” is written at the 1st byte in “graphic area”, and attribute data of nth character is written at the nth 1 byte in “Graphic area”. Attribute function is defined as follows:

Attribute RAM

1 byte

*	*	*	*	N3	N2	N1	N0
---	---	---	---	----	----	----	----

N3	N2	N1	N0	Function
0	0	0	0	Normal display
0	1	0	1	Reverse display (Text only)
0	0	1	1	Inhibit display
1	0	0	0	Blink of normal display
1	1	0	1	Blink of reverse display
1	0	1	1	Inhibit display

* : Don't care

5.5.2 Procedure of setting attribute

The example of the procedure of setting attribute is as follows:

Command	\bar{C}/D	D7	D6	D5	D4	D3	D2	D1	D0	Note
Graphic display off	1	1	0	0	0	0	*	*	*	
Graphic home address set	0	0	0	0	0	0	0	0	0	home address 1400H
	0	0	0	0	1	1	0	0	0	command
	1	0	1	0	0	0	0	1	0	
Attribute data write	0	0	0	0	0	0	0	0	0	address 1400H
	0	0	0	0	1	1	0	0	0	address pointer
	1	0	0	1	0	0	1	0	0	attribute data write
	0	0	0	0	0	0	0	0	0	command attribute
	1	1	1	0	0	0	0	0	0	data write command
	0	0	0	0	0	1	1	0	0	
	1	1	1	0	0	0	0	0	0	
	
	
Mode set	1	1	0	0	0	0	1	0	0	
Graphic display on	1	1	0	0	0	1	*	*	*	

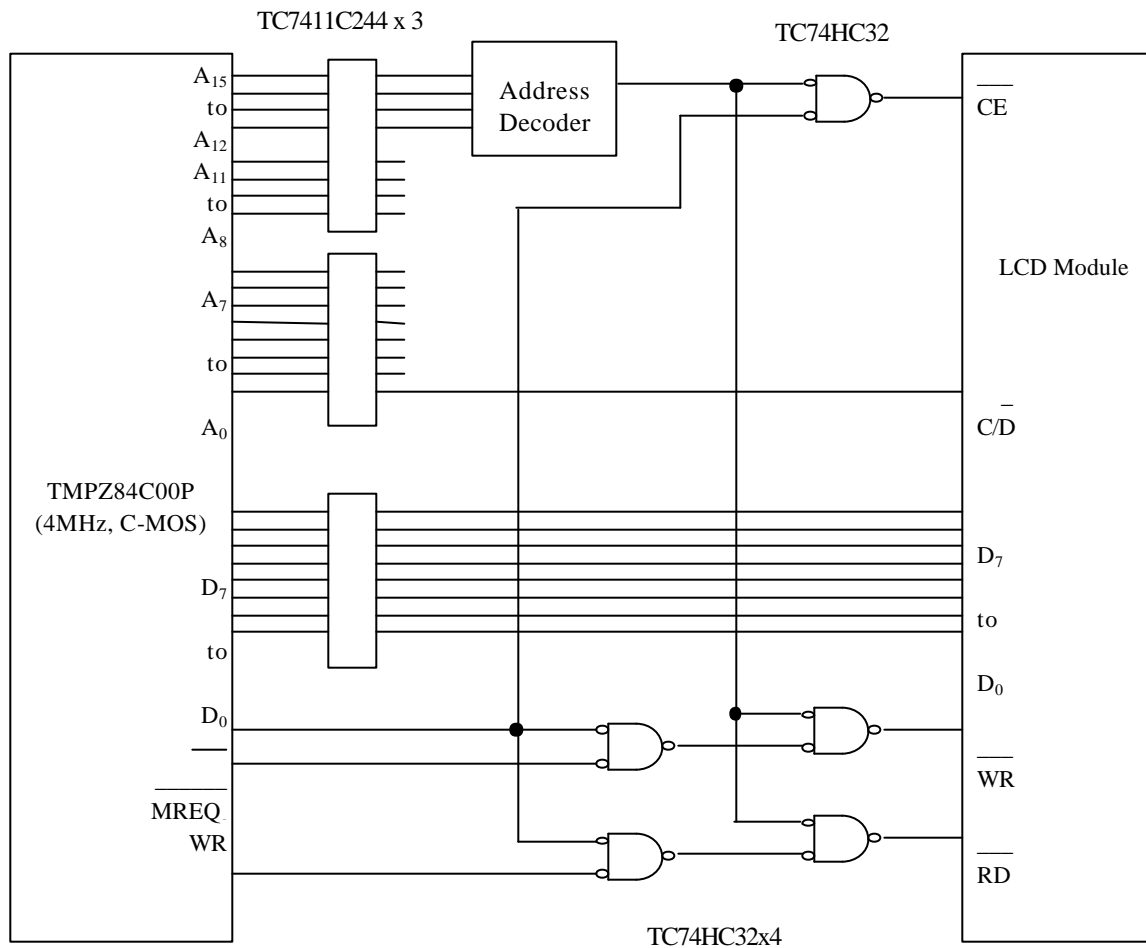
* : Don't care

6. Application Circuits

Following diagrams are the examples of interface circuit with CPU TMPZ84C00P (Z80, CMOS 4MHz). For the interface to 16 bit CPU, please refer the diagram using PPI LSI (TMP82C55).

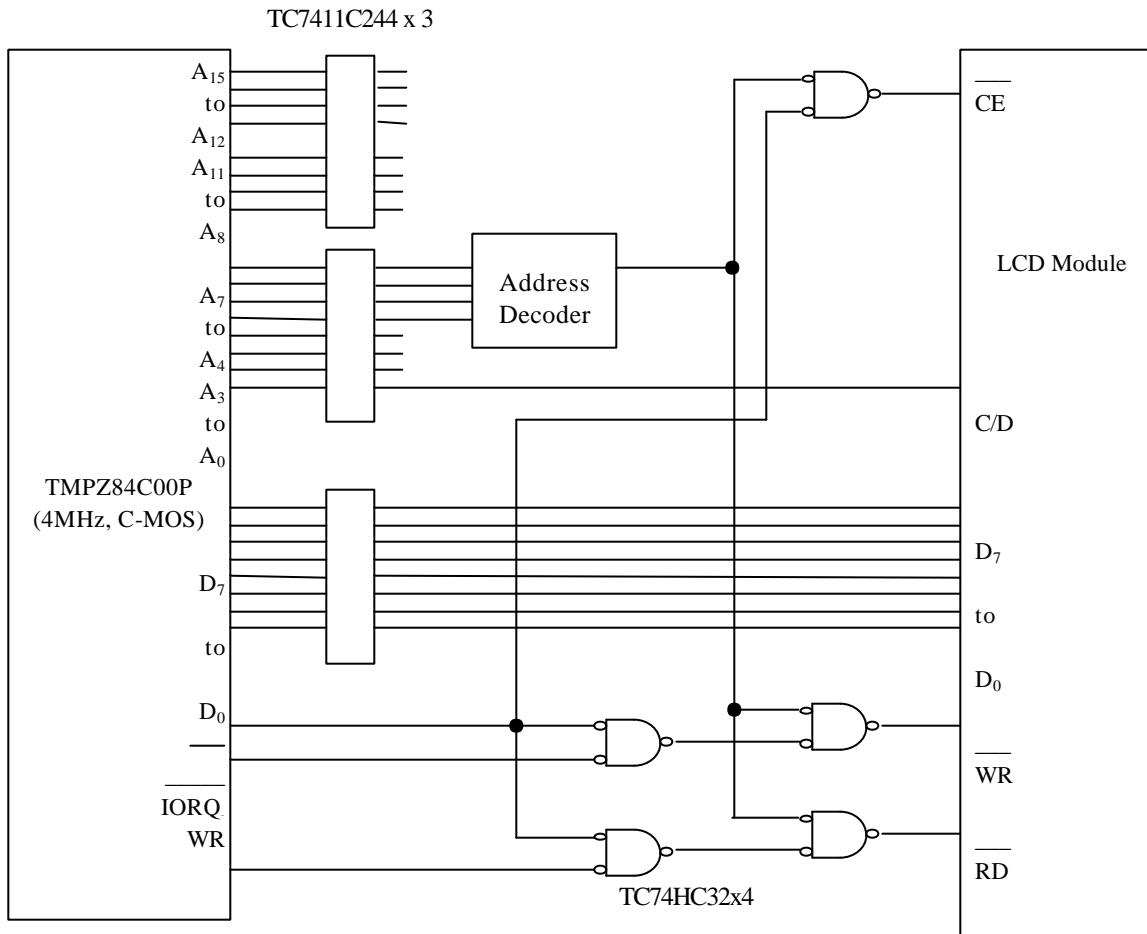
6.1 Module Located in the Memory Area of CPU

The module can be directly connected to CPU data bus as following diagram. Control signals of the module are made from MREQ, WR, RD signals of CPU, and chip select signal from address decoder. LSB of address bus (A0) can be used as C/D (command/data selection) signal.



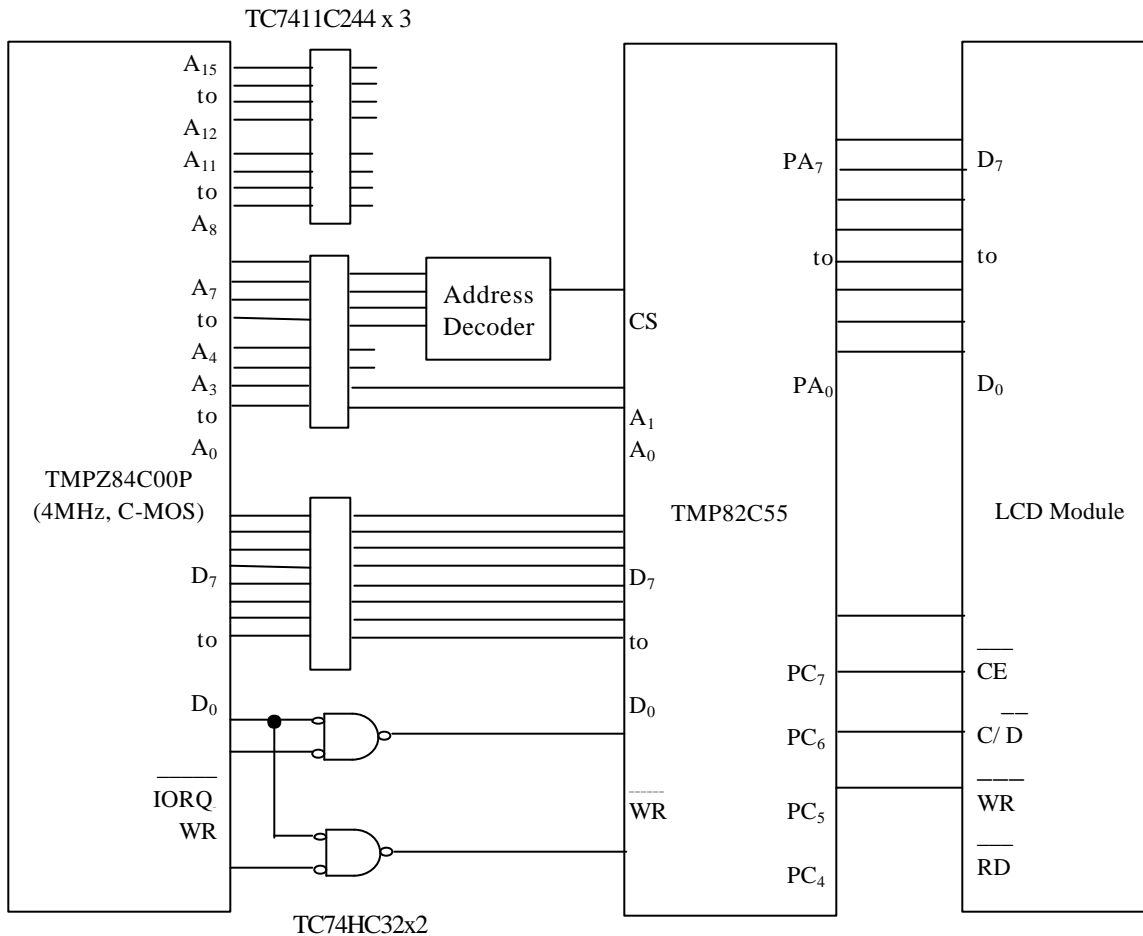
6.2 Module Located in the I/O Area of CPU

The module can be controlled as the device located in the I/O area. Control signals are made from IORQ, WR, RD of CPU, and the chop select signal from address decoder. LSB of address bus (A0) can be used as C/D (command/data selection) signal.



6.3 Interface Circuit with PPI LSI

The module can be interfaced with PPI LSI as shown in the following diagram. 8 bit data bus of the module is connected to A port of PPI, and control signals C/D, CE, WR, RD) are sent from upper 4 bit of C port. In following diagram PPI is located in the I/O address area, but interface between CPU and PPI can be left for user's design .



7. Installation

For installation of the module, please use four mounting holes located at the corners of PCB or Bezel. The Bezel is not intended to be used as a cosmetic purpose. A proper protective cover (lens) over the LCD surface and a proper enclosure are recommended to be used in order to prevent LCD surface (polarizer) from scratching or staining.

8. Cautions and Handling Precautions

8.1 Handling

- a) Refrain from strong mechanical shock or applying force to the display plane. It may cause malfunction or damage of LCD.
- b) In the case of leakage of liquid crystal material, avoid ingestion, contact of skin. If liquid crystal material sticks to skin, wash with alcohol and rinse thoroughly with water.
- c) Note that LCD surface (polarizer) is very soft as is easily damaged. Do not press the polarizer surface with hard object.
- d) The polarizer and adhesive used for lamination may be attacked by some organic solvent. When LCD surface becomes dirty wipe softly with absorbent cotton soaked in benzene.
- e) Protect the LCD module from the electro-static discharge. It will damage C-MOS LSI in the module.

8.2 Storage

- a) Do not leave the LCD module in high temperature, especially in high humidity for a long time. It is recommended to store it in the place where the temperature is between 0°C and 35°C, and where the humidity is lower than 70%.
- b) store the module without exposure to the direct sunlight.

8.3 Operation

- a) Do not connect or remove LCD module to main system with power applied.
- b) Power supplies should always be turned on before the independent input signal sources are turned on, and input signals should be turned off before power supplies are turned off.

8.4 Others

- a) Avoid condensation of water, it may cause mis-operation or corrosion of electrode.
- b) Ultraviolet ray cut filter is necessary for outdoor operation.
- c) Do not exceed the maximum ratings under the worst probable conditions with respect to supply voltage variation, input voltage variation, environmental temperature, etc.

9. Program Example

DMF-5001 DEMO 87.9.21

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```

                TITLE    DMF-5001 DEMO 87.9.21
; #####
; ###
; ###    DMF-5001 DEMO MACHINE    ###
; ###          VER. 1.0          ###
; ###    1987.9.26                ###
; ###
; #####
;
;    PROGRAM NAME : D5001.MAC
;
                .Z80
0000                ASEG
                ORG     0
0000                PA    EQU    0
0001                PB    EQU    1
0002                PC    EQU    2
0003                CW    EQU    3
0010                LCD   EQU    10H
8800                STACK EQU    8800H
2000                DATA1 EQU    2000H
4000                DATA2 EQU    4000H
6000                DATA3 EQU    6000H
A000                DATA4 EQU    0A000H
;
0000                F3
0001                31 8800                DI
                LD      SP, STACK
; 8255 MODE SET
0004                3E 82                LD      A,82H
0006                D3 03                OUT    (CW),A
;
0008                3E 80                LD      A,80H
000A                CD 016C              CALL   CWRT
;
; =====
; =====
;    MAIN ROUTINE
; =====
; =====
000D                MAIN:
000D CD 00DA                CALL   TMST ; TEXT MODE SET
0010                21 2000                LD     HL,DATA1
0013                01 0140                LD     BC,16*20
0016                MAIN10:
0016                CD 0156                CALL   SAREAD
0019                7E                    LD     A,(HL)
001A                D6 20                SUB    20H
```

```

001C CD 0178          CALL    DWRT
001F  23              INC     HL
0020  OB              DEC     BC
0021  78              LD     A,B
0022  B1              OR     C
0023  C2 0016         JP     NZ,MAIN10

;

0026  21 4000         LD     HL,DATA2
0029  01 0140         LD     BC,16*20

```

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```

002C          MAIN11:
002C CD 0156          CALL    SAREAD
002F  7E              LD     A,(HL)
0030  D6 20           SUB     20H
0032  CD 0178         CALL    DWRT
0035  23              INC     HL
0036  OB              DEC     BC
0037  78              LD     A,B
0038  B1              OR     C
0039  C2 002C         JP     NZ,MAIN11

;

003C 21 6000         LD     HL,DATA3
003F  01 0140         LD     BC,16*20
0042          MAIN12:
0042  CD 0156         CALL    SAREAD
0045  7E              LD     A,(HL)
0046  D6 20           SUB     20H
0048  CD 0178         CALL    DWRT
004B 23              INC     HL
004C 0B              DEC     BC
004D 78              LD     A,B
004E B1              OR     C
004F  C2 0042         JP     NZ,MAIN12

;

0052  3E B2           LD     A,0B2H
0054  CD 016C         CALL    CWRT          ; AUTO WRITE RESET

;

0057  CD 010D         CALL    GMSET
005A  21 A000         LD     HL,DATA4
005D 01 0A00         LD     BC,16*20*8
0060          MAIN13:
0060  CD 0156         CALL    SAREAD
0063  7E              LD     A,(HL)
0064  CD 01A4         CALL    BCG          ; DATA CHANGE
0067  CD 0178         CALL    DWRT
006A  23              INC     HL
006B 0B              DEC     BC

```

```

0063 78 LD A,B
006DB1 OR C
006E C2 0060 JP NZ,MAIN13
;
0071 3E B2 LD A,0B2H
0073 CD 016C CALL CWRT ; AUTO WRITE RESET
;
0076 16 00 LD D,0 ; COUNTER RESET
0078 MAIN50:
0078 7A LD A,D
0079 FE 00 CP 0
007B C2 0084 JP NZ,MAIN51
007E 21 0000 LD HL,0000H ; DATA1 START
0081 C3 00A4 JP MAIN60
0084 MAIN51:
0084 FE 01 CP 1
0086 C2 008F JP NZ,MAIN52
0089 21 0140 LD HL,0140H ; DATA2 START
008C C3 00A4 JP MAIN60

```

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```

008F MAIN52:
008F FE 02 CP 2
0091 C2 009A JP NZ,MAIN53
0094 21 0280 LD HL,0280H ; DATA3 START
0097 C3 00A4 JP MAIN60
009A MAIN53:
009A 3E 98 LD A,98H
009C CD 016C CALL CWRT
009F 16 00 LD D,0
00A1 C3 00BA JP MAIN20
00A4 MAIN60:
00A4 7D LD A,L
00A5 CD 0178 CALL DWRT
00A8 7C LD A,H
00A9 CD 0178 CALL DWRT
00AC 3E 40 LD A,40H ; TEXT HOME ADDRESS
00AE CD 016C CALL CWRT
;
00B1 3E 94 LD A,94H ; TEXT ON
00B3 CD 016C CALL CWRT
00B6 14 INC D
00B7 C3 00BA JP MAIN20
;-----
; SWITCH CHECK LOOP
;-----
00BA MAIN20:
00BA CD 0199 CALL SWOFF

```



```

00BD          MAIN30:
00BD 0E 01          LD      C,PB
00BF CD 01E2       CALL    INPUT
00C2 CB 47        BIT     0,A
00C4 C2 00D1       JP      NZ,MAIN40
00C7 CD 018A       CALL    SWON      ; SW ON CHECK
00CA B7           OR      A
00CB CA 00 78      JP      Z,MAIN50  ; NEXT MODE
00CE C3 00BD       JP      MAIN30

00D1          MAIN40:
00D1 01 9C40       LD      BC,40000
00D4 CD 01F4       CALL    DELAY
00D7 C3 0078       JP      MAIN50

; -----
; TMSET: TEXT MODE SET
; -----
00DA          TMSET:
00DA 3E 00          LD      A,0      ; D1
00DC CD 0178       CALL    DWRT

;
00DF 3E 00          LD      A,0      ; D2
00E1 CD 0178       CALL    DWRT

;
00E4 3E 40         LD      A,40H    ; TEXT HOME ADRS
00E6 CD 016C       CALL    CWRT

; -----
00E9 3E 14         LD      A,14H    ; D1 20

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00EB CD 0178       CALL    DWRT

;
00EE 3E 00         LD      A,0      ; D2
00F0 CD 0178       CALL    DWRT

;
00F3 3E 41         LD      A,41H    ; AREA SET
00F5 CD 016C       CALL    CWRT

; -----
00F8 3E 00         LD      A,0      ; D1
00FA CD 0178       CALL    DWRT

;
00FD 3E 00         LD      A,0      ; D2
00FF CD 0178       CALL    DWRT

;
0102 3E 00         LD      A,0      ; D2
0104 CD 016C       CALL    CWRT

; -----
0107 3E B0         LD      A,0B0H   ; AUTO WRITE SET

```

```

0109    CD 016C          CALL    CWRT
010C C9                RET
;-----
; GMSET : GRAPHIC MODE SET
;-----
010D          GMSET:
010D 3E 00          LD      A,0          ; D1
010F    CD 0178          CALL    DWRT
;
0112    3E 05          LD      A,05H         ; D2
0114    CD 0178          CALL    DWRT
;
0117    3E 42          LD      A,42H         ; GRAPHIC HOME ADRS
0119    CD 016C          CALL    CWRT
;-----
011C 3E 14          LD      A,14H         ; D1 20
011E CD 0178          CALL    DWRT
;
0121    3E 00          LD      A,0          ; D2
0123    CD 0178          CALL    DWRT
;
0126    3E 43          LD      A,43H         ; AREA SET
0128    CD 016C          CALL    CWRT
;-----
012B 3E 00          LD      A,0          ; D1
012D CD 0178          CALL    DWRT
;
0130    3E 05          LD      A,05H         ; D2
0132    CD 0178          CALL    DWRT
;
0135    3E 24          LD      A,24H         ; ADDRESS POINT SET
0137    CD 016C          CALL    CWRT
;-----
013A    3E B0          LD      A,0B0H        ; AUTO WRITE SET
013C CD 016C          CALL    CWRT
013F    C9                RET
;-----

```

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```

; SREAD: STATAS READ
;-----
0140          SREAD:
0140    F5                PUSH    AF
0141    C5                PUSH    BC
0142    D5                PUSH    DE
0143    E5                PUSH    HL

```

```

0144 3E 01          LD      A,1
0146 D3 00          OUT     (PA),A
0148                SRD00:
0148 DB 10          IN      A,(LCD)
014A E6 03          AND     3
014C FE 03          CP      3
014E C2 0148       JP      NZ,SRD00
;
0151 E1             POP     HL
0152 D1             POP     DE
0153 C1             POP     BC
0154 F1             POP     AF
0155 C9             RET
0156                SREAD:
0156 F5             PUSH    AF
0157 C5             PUSH    BC
0158 D5             PUSH    DE
0159 E5             PUSH    HL
;
015A 3E 01          LD      A,1
015C D3 00          OUT     (PA),A
015E                SARDO:
015E DB 10          IN      A,(LCD)
0160 E6 08          AND     8
0162 FE 08          CP      8
0164 C2 015E       JP      NZ,SARDO
;
0167 E1             POP     HL
0168 D1             POP     DE
0169 C1             POP     BC
016A F1             POP     AF
016B C9             RET
;
;-----
; CWRT: COMMAND WRITE
;-----
016C                CWRT:
016C CD 0140       CALL   SREAD
016F F5             PUSH    AF
0170 3E 01          LD      A,1
0172 D3 00          OUT     (PA),A
0174 F1             POP     AF
0175 D3 10          OUT     (LCD),A
0177 C9             RET
;
;-----
; DWRT: DATA WRITE
;-----

```

```

0178          DWRT:
0178    CD 0140          CALL    SREAD
017B          DWRT0:
017B F5          PUSH    AF
017C 3E 00          LD      A,0
017E D3 00          OUT    (PA),A
0180    F1          POP     AF
0181    D3 10          OUT    (LCD),A
0183    C9          RET

;
0184          DWRT2:
0184    CD 0156          CALL    SAREAD
0187    C3 017B          JP     DWRT0

;-----
; SWON: MANUAL SW ON CHECK
;-----

018A          SWON:
018A    0E 01          LD      C,PB
018C CD 01E2          CALL    INPUT
018F    CB 4F          BIT    1,A
0191    CA 0197          JP     Z,SWON0
0194    3E FF          LD      A,0FFH
0196    C9          RET
0197          SWON0:
0197    AF          XOR A
0198    C9          RET

;-----
; SWOFF: MANUAL SW OFF CHECK
;-----

0199          SWOFF:
0199    0E 01          LD      C,PB
019B CD 01E2          CALL    INPUT
019E CD 4F          BIT    1,A
01A0    CA 0199          JP     Z,SWOFF
01A3    C9          RET

;-----
; BIT CHANGE
;-----

01A4          BCG:
01A4    C5          PUSH    BC
01A5    06 00          LD      B,0
01A7    CB 47          BO:    BIT    0,A
01A9    CA 01AE          JP     Z,B1
01AC    CB F8          SET    7,B
01AE    CB 4F          B1:    BIT    1,A
01B0 CA 01B5          JP     Z,B2
01B3 CB F0          SET    6,B
01B5 CB 57          B2:    BIT    2,A

```

```

01B7 CA 01BC      JP      Z,B3
01BA   CB E8      SET      5B
01BC   CB 5F      BIT      3,A
01BE CA 01C3      B3:    JP      Z,B4
01C1 CB E0        SET      4,B
01C3 CB 67        B4:    BIT      4,A
01C5 CA 01CA      JP      Z,B5

```

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```

01C8 CB D8        SET      3,B
01CA   CB 6F      B5:    BIT      5,A
01CC   CA 01D1      JP      Z,B6
01CF CB D0        SET      2,B
01D1 CB 77        B6:    BIT      6,A
01D3 CA 01D8      JP      Z,B7
01D6 CB C8        SET      1,B
01D8 CB 7F        B7:    BIT      7,A
01DA   CA 01DF      JP      Z,B8
01DD   CB C0        SET      0,B
01DF                                B8:
01DF   78                                LD      A,B
01E0 C8                                POP     BC
01E1 C9                                RET

```

```

;-----
; INPUT: C: PORT ADDRESS
;-----

```

```

01E2      INPUT:
01E2 C5      PUSH   BC
01E3 D5      PUSH   DE
01E4      INPUT1:
01E4 06 01      LD     B,10
01E6 ED 78      IN    A,(C)
01E8 57        LD    D,A
01E9      INPUT2:
01E9 ED 78      IN    A,(C)
01EB BA        CP    D
01EC C2 01E4    JP    NZ,INPUT1
01EF 10 F8      DJNZ  INPUT2
01F1   D1      POP    DE
01F2   C1      POP    BC
01F3   C9      RET

```

```

;-----
; DELAY: BC LOOP CNT
; (171*BC+44)*.25*10^-6 (SEC)
;-----

```

```

01F4      DELAY:
01F4   C5      PUSH   BC
01F5   D5      PUSH   DE

```

```

01F6 1E10 DEL1: LD E,10H
01F8 1D DEL2: DEC E
01F9 C2 01F8 JP NZ,DEL2
01FC 0B DEC BC
01FD 78 LD A,B
01FE B1 OR C
01FF C2 01F6 JP NZ,DEL1
0202 D1 POP DE
0203 C1 POP BC
0204 C9 RET

```

```

0205 00 00 00 00 DEFB 0, 0, 0, 0

```

END

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Macros:

Symbols:

B0	01A7	B1	01AE	B2	01B5	B3	01BC
B4	01C3	B5	01CA	B6	01D1	B7	01D8
B8	01DF	BCG	01A4	CW	0003	CWRT	016C
DATA1	2000	DAT2	4000	DATA3	6000	DATA4	A000
DEL1	0AF6	DEL2	01F8	DELAY	01F4	DWRT	0178
DWRT0	017B	DWRT2	0184	GMSET	010D	INPUT	01E2
INPUT1	01E4	INPU2	01E9	LCD	0010	MAIN	000D
MAIN10	0016	MAIN11	002C	MAIN12	0042	MAIN13	0060
MAIN20	00BA	MAIN30	00BD	MAIN40	00D1	MAIN50	0078
MAIN51	0084	MAIN52	008F	MAIN53	009A	MAIN60	00A4
PA	0000	PB	0001	PC	0002	SARD0	015E
SAREAD	0156	SRD00	0148	SREAD	0140	STACK	8800
SWOFF	0199	SWON	018A	SWON0	0197	TMSET	00DA

No Fatal error(s)

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